

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-20 are presently active in this case, Claims 1-14 having been amended by way of the present amendment.

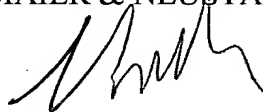
Support for the present amendment may be found, for example, at page 6, lines 19-27 of the specification. The Applicant therefore respectfully submits that no new matter has been added by way of the present amendment.

In response to the Restriction Requirement dated April 26, 2002, the Applicant elects without traverse the invention of Group I and identifies amended Claims 1-14 as readable on the elected invention.

Accordingly, an early and favorable action is respectfully requested.

Respectfully submitted,

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IN THE TITLE

At page 1, lines 1-2, please delete the title in its entirety and substitute therefor:
[SPIRAL INDUCTOR AND METHOD FOR FABRICATING SEMICONDUCTOR
INTEGRATED CIRCUIT DEVICE HAVING SAME]
SEMICONDUCTOR DEVICE WITH SPIRAL INDUCTOR AND METHOD FOR
FABRICATING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

IN THE CLAIMS

1. (Once Amended) A [spiral inductor] semiconductor device comprising:
a substrate;
a protruding portion which is formed on the top face of the substrate and the top of
which serves as a dummy element for controlling a chemical mechanical polishing process;
and
a conductive layer which is formed on the substrate so as to have a spiral shape and
which serves as an induction element,
wherein said protruding portion is formed in a region other than a region directly
below said conductive layer.
2. (Once Amended) A [spiral inductor] semiconductor device as set forth in claim 1,
wherein the substrate is an SOI substrate, and

said protruding portion is formed of an SOI layer of said SOI substrate.

3. (Once Amended) A [spiral inductor] semiconductor device as set forth in claim 2, wherein the substrate includes an N-type semiconductor layer.

4. (Once Amended) A [spiral inductor] semiconductor device as set forth in claim 2, wherein the substrate includes a P-type semiconductor layer.

5. (Once Amended) A [spiral inductor] semiconductor device comprising:

a substrate;

a protruding portion which is formed on the top face of the substrate and the top of which serves as a dummy element for controlling a chemical mechanical polishing process;

a conductive layer which is formed on the substrate so as to have a spiral shape and which serves as an induction element; and

a protective film which is formed between the substrate and said conductive layer and prevents silicidation of said protruding portion.

6. (Once Amended) A [spiral inductor] semiconductor device as set forth in claim 5, wherein the substrate is an SOI substrate, and

said protruding portion is formed of an SOI layer of said SOI substrate.

7. (Once Amended) A [spiral inductor] semiconductor device as set forth in claim 6, which further comprises an extracting wiring which is connected to said conductive layer.

8. (Once Amended) A [spiral inductor] semiconductor device as set forth in claim 6, wherein the substrate includes an N-type semiconductor layer.

9. (Once Amended) A [spiral inductor] semiconductor device as set forth in claim 6, wherein the substrate includes a P-type semiconductor layer.

10. (Once Amended) A [spiral inductor] semiconductor device as set forth in claim 5, wherein said protruding portion is formed in a region other than a region directly below said conductive layer.

11. (Once Amended) A [spiral inductor] semiconductor device as set forth in claim 10, wherein the substrate is an SOI substrate, and

said protruding portion is formed of an SOI layer of said SOI substrate.

12. (Once Amended) A [spiral inductor] semiconductor device as set forth in claim 11, which further comprises an extracting wiring which is connected to said conductive layer.

13. (Once Amended) A [spiral inductor] semiconductor device as set forth in claim 11, wherein the substrate includes an N-type semiconductor layer.

14. (Once Amended) A [spiral inductor] semiconductor device as set forth in claim 11, wherein the substrate includes a P-type semiconductor layer.